Patent claims

1. A reconfigurable architecture for a computer device having at least one individually configurable and/or reconfigurable sequential circuit which has a stage containing inputs and a stage containing outputs, where output variables from at least some of the outputs at a time t_{n-1} form the input variables on associated inputs of the sequential circuit at a time t_n and where means are provided for clock-controlled storage of the output variables from the sequential circuit between the times t_{n-1} and t_n.

2. The architecture as claimed in claim 1, characterized in that the storage means are register memory elements.

3. The architecture as claimed in claim 1 or 2, characterized by a three-stage design for the sequential circuit with three stages being connected in series.

4. The architecture as claimed in claim 3, characterized
- by a first stage comprising a plurality of parallel-connected memory elements which can be addressed via input lines, each memory element being able to be supplied with a subset of the input variables attached to an associated, ascertained implicant,
- by a second stage, connected downstream of the first stage, with memory elements which can be addressed by the identifiers of the individual implicants,

and
- by a third stage, connected downstream of the second stage, with means for disjunctive logic combination of the output values from the individual implicants from the memory elements in the second stage.

5. The architecture as claimed in claim 4, characterized by ascertainment of the implicants using minimization methods.

6. The architecture as claimed in claim 4 or 5, characterized in that the first stage is logically combined with the second stage by means of at least one crossbar switch.

7. The architecture as claimed in one of the preceding claims, characterized by CAMs and/or RAMs as memory elements.

8. The architecture as claimed in one of the preceding claims, characterized by integration of at least one GCA.

9. The architecture as claimed in one of the preceding claims, characterized by magnetoresistive memory elements, particularly of the TMR type.